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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER FINDLEY, CHRISTOPHER G	
			ART UNIT	PAPER NUMBER
			2621	
			NOTIFICATION DATE	DELIVERY MODE
			05/13/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/711,139	Applicant(s) JU, CHI-CHENG	
	Examiner CHRISTOPHER FINDLEY	Art Unit 2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 January 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/22/2009 have been fully considered but they are not persuasive.
2. Re claim 1, the Applicant contends that both Diaz' and Miyawaki's disclosures are silent on any correlation between the video encoding and the video decoding, not to mention using an encoder to encode an encoding bit stream according to characteristics of a decoding bit stream to be decoded by a decoder. However, the Examiner respectfully disagrees. As noted by the Applicant, Miyawaki discloses that the video encoder converts the digital image output of the image decoder into video signals such as NTSC or PAL video signals that are displayed on a standard television set (Miyawaki: column 7, line 64-column 8, line 1). NTSC and PAL signals are incompatible with each other, meaning that an NTSC decoder has unique characteristics in relation to a PAL decoder, and vice versa. By encoding the video signal into either of the formats listed, the encoder of Miyawaki encodes the data according to characteristics of a decoding bit stream to be decoded by a decoder.
3. Therefore, the Examiner maintains the previous rejection, and this action is made final accordingly.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al. (US 5812789 A) in view of Miyawaki et al. (US 5752266 A).

Re **claim 1**, Diaz discloses a video signal processing system for encoding an encoding bit stream according to characteristics of a decoding bit stream, the encoding and decoding bit streams include a plurality of encoding schemes, the video signal processing system comprising: a storage device utilized for storing data of the decoding bit stream and the encoding bit stream (Diaz: Fig. 2, memory 50); and an encoder electrically connected to the storage device for encoding the encoding bit stream according to an encoding scheme of the decoding bit stream (Diaz: Fig. 2, encoder 46), the memory bandwidth needed for a third encoding scheme out of the plurality of encoding schemes being greater than the memory bandwidth needed for any other encoding scheme out of the plurality of encoding schemes (Diaz: column 3, lines 26-39, some images are decoded based on previous images (P frames) and some images are decoded based previous and future images (B frames), wherein more memory bandwidth would be required for accessing two images as opposed to just one image)

Diaz does not specifically disclose the encoder encoding the encoding bit stream using one of the plurality of encoding schemes except the third encoding scheme when the encoding scheme of the decoding bit stream is the third encoding scheme.

However, Miyawaki discloses a system and method of controlling memory access operations by changing respective priorities thereof, based on situation of the memory,

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wherein the memory control circuit may arbitrate and schedule the memory access operations of writing and reading the coded data and decoded image data to and from the dynamic random access memory as well as a memory access operation of refreshing the dynamic random access memory (Miyawaki: column 3, lines 22-26). Furthermore, Miyawaki discloses that the memory controller may change the priority of different data types (Miyawaki: column 3, lines 8-15), which one of ordinary skill in the art at the time of the invention would have found obvious to include various picture types (i.e., I-, P-, and B-frames) since the system disclosed by Miyawaki relates to processing MPEG data (Miyawaki: column 5, lines 25-32). Therefore, the lower priority operations (i.e., writing coded data to the memory) utilize the memory access bandwidth left-over from the higher priority operations (i.e., decoding coded data stored in the memory) by prioritizing the data which best fits into said left-over bandwidth. Since both Diaz and Miyawaki relate to controlling memory access for shared memory, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the data prioritization of Miyawaki with the codec device of Diaz in order to realize an efficient memory system without increasing the capacity of a buffer or memory, the width of a memory bus, or an operating frequency (Miyawaki: Abstract section).

Re **claim 2**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 2, as discussed above in claim 1. Additionally, Diaz discloses that the plurality of encoding schemes include three encoding schemes, and in addition to

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the third encoding scheme, the three encoding schemes further include a first encoding scheme and a second encoding scheme (Diaz: column 7, lines 16-22).

Re **claim 3**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 3, as discussed above in claim 2. Additionally, Diaz discloses that the memory bandwidth needed for the first encoding scheme is less than the memory bandwidth needed for the second encoding scheme, and the memory bandwidth needed for the second encoding scheme is less than the memory bandwidth needed for the third encoding scheme (Diaz: column 7, lines 16-22, intra coded images (I frames) do not require access to the stored images, so they use no memory bandwidth; column 3, lines 26-39, some images are decoded based on previous images (P frames) and some images are decoded based previous and future images (B frames), wherein more memory bandwidth would be required for accessing two images as opposed to just one image).

Re **claim 4**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 4, as discussed above in claim 3. Additionally, Diaz discloses that the first, second, and third encoding schemes are the intra encoding, the predictive encoding, and the bidirectionally predictive encoding, respectively (Diaz: column 7, lines 16-22).

Re **claim 5**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 5, as discussed above in claim 4. Additionally, Diaz discloses that when the encoding scheme of the decoding bit stream is the intra encoding, the encoding scheme of the encoding bit stream is one of the intra encoding, the predictive

encoding, and the bidirectionally predictive encoding (Diaz: column 8, lines 19-29, MPEG inherently utilizes one of intra, predicted, or bidirectionally predicted coding modes).

Re **claim 6**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 6, as discussed above in claim 4. Additionally, Diaz discloses that when the encoding scheme of the decoding bit stream is the predictive encoding, the encoding scheme of the encoding bit stream is one of the intra encoding, and the predictive encoding (Diaz: column 8, lines 19-29, MPEG inherently utilizes one of intra, predicted, or bidirectionally predicted coding modes; column 3, lines 26-39, dropping frames to reduce required memory bandwidth).

Re **claim 7**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 7, as discussed above in claim 4. Additionally, Diaz discloses that when the encoding scheme of the decoding bit stream is the bidirectionally predictive encoding, the encoding scheme of the encoding bit stream is the intra encoding (Diaz: column 8, lines 19-29, MPEG inherently utilizes one of intra, predicted, or bidirectionally predicted coding modes; column 3, lines 26-39, dropping frames to reduce required memory bandwidth).

Re **claim 8**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 8, as discussed above in claim 1. Additionally, Diaz discloses that the storage device is a memory (Diaz: Fig. 2, memory 50), and the video signal processing system further comprises a memory interface for controlling access to the memory (Diaz: Fig. 2, memory interface 48).

Re **claim 9**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 9, as discussed above in claim 1. Additionally, Diaz discloses a decoder electrically connected to the storage device for decoding the decoding bit stream (Diaz: Fig. 2, decoder 44) and sending the encoding scheme of the decoding bit stream to the encoder (Diaz: column 8, lines 19- 29, the decoder/encoder is capable of utilizing multiple coding standards; column 6, lines 32-38, the type of coding standard factors into bandwidth calculations; column 6, lines 12-13, the DMA engine may be an integrated part of the decoder/encoder).

Re **claim 10**, Diaz discloses a video signal encoding and decoding method for encoding an encoding bit stream according to characteristics of a decoding bit stream, the encoding and decoding bit streams include a plurality of encoding schemes, the video signal encoding and decoding method comprising: (a) checking an encoding scheme of the decoding bit stream to decide an encoding scheme for encoding the encoding bit stream (Diaz: column 8, lines 19-29, the decoder/encoder is capable of utilizing multiple coding standards; column 6, lines 32-38, the type of coding standard factors into bandwidth calculations; column 6, lines 12-13, the DMA engine may be an integrated part of the decoder/encoder).

Diaz discloses that intra coded images (I frames) do not require access to the stored images, so they use no memory bandwidth (column 7, lines 16-22) and some images are decoded based on previous images (P frames) and some images are decoded based previous and future images (B frames) (column 3, lines 26-39), wherein more memory bandwidth would be required for accessing two images as opposed to

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just one image, but Diaz does not specifically disclose encoding the encoding bit stream using one of the plurality of encoding schemes except a third encoding scheme when the encoding scheme of the decoding bit stream is the third encoding scheme, the memory bandwidth needed for the third encoding scheme being greater than the memory bandwidth needed for any other encoding scheme out of the plurality of encoding schemes. However, Miyawaki discloses a system and method of controlling memory access operations by changing respective priorities thereof, based on situation of the memory, wherein the memory control circuit may arbitrate and schedule the memory access operations of writing and reading the coded data and decoded image data to and from the dynamic random access memory as well as a memory access operation of refreshing the dynamic random access memory (Miyawaki: column 3, lines 22-26). Furthermore, Miyawaki discloses that the memory controller may change the priority of different data types (Miyawaki: column 3, lines 8-15), which one of ordinary skill in the art at the time of the invention would have found obvious to include various picture types (i.e., I-, P-, and B-frames) since the system disclosed by Miyawaki relates to processing MPEG data (Miyawaki: column 5, lines 25-32). Therefore, the lower priority operations (i.e., writing coded data to the memory) utilize the memory access bandwidth left-over from the higher priority operations (i.e., decoding coded data stored in the memory) by prioritizing the data which best fits into said left-over bandwidth. Since both Diaz and Miyawaki relate to controlling memory access for shared memory, one of ordinary skill in the art at the time of the invention would have found it obvious to combine the data prioritization of Miyawaki with the codec device of Diaz in order to

realize an efficient memory system without increasing the capacity of a buffer or memory, the width of a memory bus, or an operating frequency (Miyawaki: Abstract section)

Claim 11 has been analyzed and rejected with respect to claim 2 above.

Claim 12 has been analyzed and rejected with respect to claim 3 above.

Claim 13 has been analyzed and rejected with respect to claim 4 above.

Claim 14 has been analyzed and rejected with respect to claim 5 above.

Claim 15 has been analyzed and rejected with respect to claim 6 above.

Claim 16 has been analyzed and rejected with respect to claim 7 above.

Re **claim 17**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 17, as discussed above in claim 10. Additionally, Diaz discloses that the decoding bit stream and the encoding bit stream are both accessed through the same memory interface circuit corresponding to a memory (Diaz: Fig. 2, decoder 44 and encoder 46 are both connected to memory 50 via the memory interface 48 and the DMA engine 52).

Re **claim 18**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 18, as discussed above in claim 10. Additionally, Diaz discloses that the encoding bit Stream is an encoding bit stream corresponding to a picture (Diaz: Fig. 2, video decoding circuit 12 and video encoding circuit 62 process video data, which corresponds to sequences of pictures).

Re **claim 19**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 19, as discussed above in claim 10. Additionally, Diaz discloses

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that the encoding bit stream is an encoding bit stream corresponding to a block of a picture (Diaz: column 8, lines 19-29, MPEG inherently provides for processing video in blocks of pixels).

Re **claim 20**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 20, as discussed above in claim 19. Additionally, Diaz discloses that the block is a macroblock (Diaz: column 8, lines 19-29, MPEG inherently provides for processing video in macroblocks of 16X16 pixels).

Claim 21 has been analyzed and rejected with respect to claim 5 above.

Re **claim 22**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 22, as discussed above in claim 21. Additionally, Diaz discloses encoding the block according to the intra encoding when the encoding scheme of the picture is the intra encoding (Diaz: column 8, lines 19-29, MPEG inherently utilizes one of intra, predicted, or bidirectionally predicted coding modes).

Re **claim 23**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 23, as discussed above in claim 21. Additionally, Diaz discloses encoding the block according to one of the intra encoding and the forward motion compensation encoding when the encoding scheme of the picture is the predictive encoding (Diaz: column 8, lines 19-29, MPEG inherently utilizes one of intra, predicted, or bidirectionally predicted coding modes).

Re **claim 24**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 24, as discussed above in claim 21. Additionally, Diaz discloses encoding the block according to one of the intra encoding, the forward motion

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compensation encoding, the backward motion compensation encoding, and the bidirectional motion compensation encoding when the encoding scheme of the picture is the bidirectionally predictive encoding (Diaz: column 8, lines 19-29, MPEG inherently utilizes one of intra, predicted, or bidirectionally predicted coding modes).

Re **claim 25**, the combined system of Diaz and Miyawaki discloses a majority of the features of claim 25, as discussed above in claim 21. Additionally, Diaz discloses encoding the block according to one of the forward motion compensation encoding, the backward motion compensation encoding, and the bidirectional motion compensation encoding when the encoding scheme of the picture is the bidirectionally predictive encoding (Diaz: column 8, lines 19-29, MPEG inherently utilizes one of intra, predicted, or bidirectionally predicted coding modes).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- a. Memory management for an MPEG2 compliant decoder; Cheney et al. (US 5668599 A)
- b. Methods and apparatus for processing luminance and chrominance image data; Pearlstein et al. (US 6385248 B1)
- c. System and method for adaptive video processing with coordinated resource allocation; Rodriguez et al. (US 20020009149 A1)

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d. Recording apparatus and coding apparatus; Fukuda et al. (US 6856759 B1)

e. Moving image encoding method and apparatus, and moving image decoding method and apparatus; Kato (US 6415055 B1)

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER FINDLEY whose telephone number is (571)270-1199. The examiner can normally be reached on Monday-Friday (8:30 AM-5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on 571-272-7905. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marsha D. Banks-Harold/
Supervisory Patent Examiner, Art Unit 2621

/Christopher Findley/